鋰電池保護IC Delay Time 定義說明 正確說的

Reported FAE Dept.

Dec. 12th 2022





Customer:

What is the root cause of delay time over maximum spec during SCP test?

Ans:

According to this waveform, we can only see that battery pack (P+) was turned off by DFET after short circuit, but cannot understand the real tshort time.

The definition of tshort is

2 High start from V- rise to Vshort (0.185V) until DOUT start falling to logic low.

Please see the timing chart in page 3.

Short Protection Voltage	Vshort	Detect rising edge of 'V-' pin voltage	0.180	0.185	0.190	V	F
Delay Time for Short Protection	tshort	V_{DD} =3.0V, V-=0V to 0.50V	210	280	350	μs	F







(2) Over-discharge, Excess discharge current, Short circuit







Customer:

What is reason that SCP protection time is 576us, but not within 350us?

Ans:

tshort is the definition of IC behavior, your waveform is battery pack (system) level measurement.

The time scale is microsecond level, delay time is easily longer than IC measurement level.

Also, a part of delay relates to MOSFET.

According to the correct measurement, tshort is within the spec. Please see the detail in page 5 and page 6.

For total battery pack point of view, it is better to evaluate the SCP delay time with whole circuit.





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1 High	1.752 A	1.277	677.0m	1.752	546.9m					
1 Low	13.67mA	-45.62m	-161.4m	13.67m	82.51m					
2 High	3.860 V	1.038	77.19m	3.860	1.647		<u> </u>	2.50MS/c		<u> </u>
2 Low	40.16mV	47.04m	14.84m	64.69m	15.67m	-400μs -48.0	0000us	10k points		- 300MA
3 Low	3.646 V	3.684	3.495	3.718	59.34m					
4 High	3.811 V	1.935	56.72m	3.811	2.166				1	6 Nov 2022)
4 Low	32.81mV	33.87m	5.625m	70.00m	26.78m				1	7:19:27





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	4 Low	32.81mV	33.87m	5.625m	70.00m	26.78m	17:19:27





